Secure Embedded Systems

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Abstract

Department of Defense (DoD) systems are increasingly the targets of deliberate and sophisticated attacks. In order to assure mission success, military systems must be entrusted to perform its intended functions, prevent attacks, and even operate with resilience under attack. DoD has thus directed that cyber security must be integrated into system life cycles [1], the practice of securing a system after it has been designed is no longer acceptable. However, the co-design of security with functionality has to overcome a major challenge; rarely can the security requirements be accurately identified when the design begins.

This paper gives an overview on Lincoln Laboratory's co-design methodology for secure embedded systems, which consists of an architecture that decouples secure and functional design aspects and a few enabling technologies. This architecture uses cryptography to ensure the confidentiality and integrity of an embedded system being designed. The development of a hypothetical secure embedded system for an unmanned aerial system (UAS) is used to illustrate our co-design methodology. We will also briefly describe our ongoing effort in adding resiliency to a secure embedded system so that it can continue to function under attack for enhanced availability.

Introduction

Lincoln Laboratory is at the research and development (R&D) forefront of leading edge signal processing solutions for challenging critical missions. Many of Lincoln Laboratory's prototype embedded systems must be designed with security in mind, so that they can be quickly brought into compliance with DoD's relevant requirements to support field tests and technology transfers. DoD has now directed that cyber security must be co-developed with mission capabilities and not be treated as an "after-thought," since any after-the-fact system changes could be prohibitively expensive or even impossible [1]. The co-design of embedded system functionality with its security is difficult as rarely can the security requirements be accurately identified when the design process starts. Also, embedded system engineers tend to focus on well-understood functional capabilities rather than obscure security requirements.

The security requirements of an embedded system are determined according to its concept of operations (CONOPS). Security aims at preventing attacks so that a system can be entrusted to perform in support of a successful mission. For critical mission functions, we may need to go a step further and provide resiliency that enables the system to continue functioning, albeit with possibly degraded capabilities, when security fails.

34 The goals of securing a system can be summarized as the assuring of confidentiality, integrity, and
35 availability, which is often referred to as the CIA triad. We define the CIA triad of an embedded system
36 as follows:

37 • Confidentiality assures that its critical information, such as application code and surveillance
38 data, will not be disclosed to unauthorized entities.
39 • Integrity assures that the system operation cannot be altered.
40 • Availability assures that mission objectives cannot be disrupted.

41 Security must be provided with minimal impacts on the system's size, weight, power, and cost (SWaP-C)
42 and development schedule. In addition, the design must consider usability as valid secure systems must
43 also be practical and usable.

44 The objective of this paper is to provide an overview of Lincoln Laboratory's secure embedded system
45 development methodology and its enabling technologies. We use the development of a hypothetical
46 secure unmanned aerial system (UAS) embedded system as an example to illustrate how we use
47 cryptography to ensure confidentiality and integrity. Using this example, we demonstrate the
48 identification of potential attacks by considering its CONOPS, countermeasures to these attacks, and
49 discuss the design and implementation of a cryptography-based security architecture. We will also
50 overview ongoing work to extend the methodology and provide the resiliency required for availability,
51 which is not provided by cryptography itself.

52 A comprehensive security technology survey is beyond the scope of this paper. Instead, we introduce a
53 number of relevant security technologies that Lincoln Laboratory has been developing to address
54 existing technology gaps in the security of embedded systems.

Challenges in Securing Embedded Systems

56 An embedded system is a computer system designed for a dedicated function. This is in contrast to a
57 general-purpose computer system (e.g., a desktop computer). A major objective of creating an
58 embedded system for a specific task is to optimize it for better performance in terms of smaller form
59 factor, lower power consumption, higher throughput, etc. As such, an embedded system will provide
60 very little, if any, SWaP allowance for security. Security thus must not impose excessive overheads on
61 the system they are protecting.

62 Every year DoD acquires and operates numerous embedded systems, ranging from intelligence,
63 surveillance, and reconnaissance (ISR) sensors to electronic warfare/electronic signal intelligence
64 (EW/ELINT) applications [1]. Depending on their objective mission CONOPS, embedded systems have
65 different security requirements. For example, a system planned for contiguous United States (CONUS)
66 deployment could have lower security requirements than a system for forward operating base (FOB)
67 operation, since the latter are deployed to support tactical operations. Any methodology for securing
68 embedded systems should be customizable to meet CONOPS needs.

69 It is interesting to note that while DoD has some of the most demanding applications, in terms of
70 throughput and SWaP-C, the time that DoD drives technology development has long passed. Instead,
71 DoD now strives to leverage commercial technologies, which are driven by computing, communications,
72 and gaming industries. The result is that the critical technology in a system is often its software and/or
73 firmware, which define the system functionality, rather than the processor hardware itself. Security
74 technologies must be compatible with embedded systems using COTS (commercial-off-the-shelf)
75 processor hardware platforms.

76 As military electronic systems continue to increase in sophistication and capability, the cost and
77 development time of these systems also grow. The use of open systems architecture (OSA) can improve
78 the development and lifecycle efficiency of asset procurements. DoD has thus directed that all DoD
79 components and agencies use OSA for acquisition [3]. OSA uses industry consensus, non-proprietary,
80 system architectural standards so that variable payloads can be shared among variable platforms.
81 Competition for technology refresh and enterprise-level acquisition are thus promoted. However,
82 adding security to OSA, if not well-thought-out, could interfere with its openness. As most current
83 security approaches are ad-hoc, proprietary, and expensive, they are incompatible with OSA principles,
84 especially when each component individually implements and manages its own security. A system level
85 secure architecture that will seamlessly work with various OSA components is a challenge.

86 The current trends of how DoD acquires its embedded systems require new thinking on their
87 development for security. We will explain the secure embedded system design methodology that
88 Lincoln Laboratory has developed to address the challenges in securing DoD embedded systems.

Design Process

90 Figure 1 captures the design process of a secure embedded system with the steps dedicated to security
91 highlighted. CONOPS is developed from the mission objectives and used to derive both functional and
92 security requirements. An initial system design is created, evaluated, and implemented. While
93 functionality and security must be co-developed, it is desirable to decouple their implementations so
94 that the interference of security to the test and evaluation of functionality is minimized. Note that
95 several design iterations may be required before the mission objectives are met.

96 We use the design of a hypothetical small unmanned aerial system (UAS) for a video surveillance
97 application to illustrate the secure embedded system design process. The CONOPS of this example UAS
98 application is as follows. At startup, the UAS is provisioned on the ground by loading its long term
99 credentials for identification and authentication purposes. Mission specific software and firmware,
100 which are considered to be critical program information (CPI) as they contain information on
101 destinations, targets, search and track algorithms, etc., are loaded into their respective memories. The
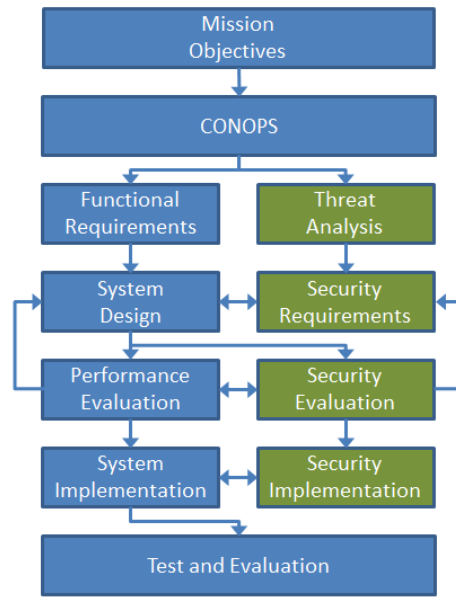102 system is then booted up and prepared for execution.

Figure 1: Secure embedded system design process.

Figure 2 illustrates the embedded system in its execution phase. Under the command and control of a ground control station (GCS), the UAS takes off, flies to destination, and begins to collect video data. Target information obtained by processing video data is encrypted and broadcasted to authorized ground stations using the radio. Raw video data are also saved in the storage for further processing after landed. At shutdown, both raw and processed video data are considered to be sensitive and must have been saved securely. Finally, when the system is off, any persistent state, such as the long-term credentials, must be protected.
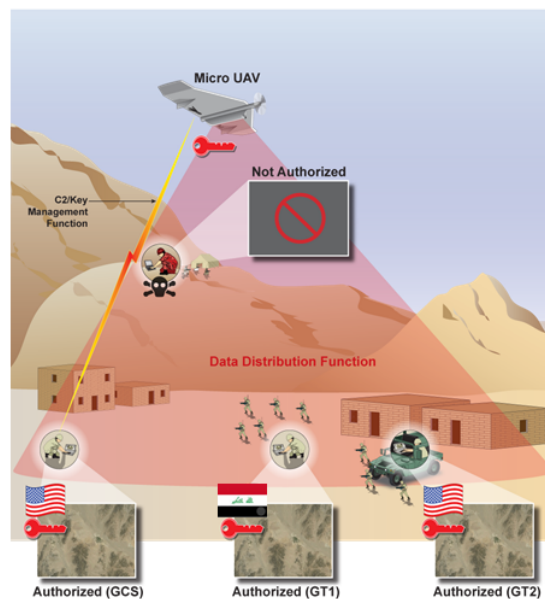

Figure 2: Example UAS application in its execution phase.

114 Figure 3 shows a high-level architecture initially designed for the functionality of this example UAS
115 embedded system. It consists of a central processing unit (CPU) and a field programmable gate array
116 (FPGA) interconnected with an Ethernet network. The CPU will be provided with its basic input/output
117 system (BIOS), operating system (OS), and mission specific application code in memory. The FPGA has its
118 configuration stored in a firmware memory. Besides a video camera payload, the system also has
119 memory, storage, and radio, which are accessible by the CPU and/or FPGA through Ethernet. The CPU
120 handles command and control received through the radio. The video signal is first processed by the
121 FPGA (e.g., for target detection and identification) and then passed to the CPU for information
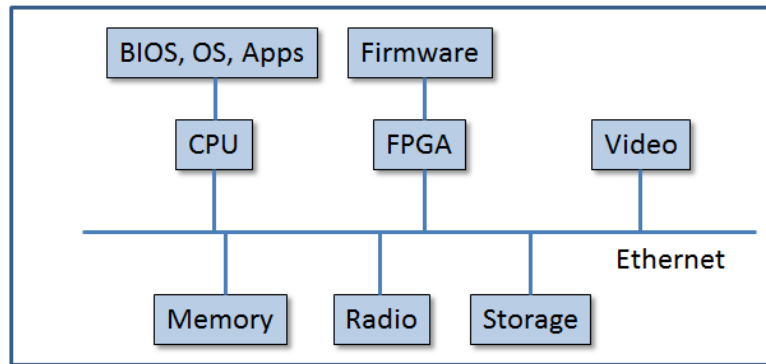122 extraction (e.g., target tracking).

123

124 **Figure 3: Example UAS embedded system functional architecture.**

125 High performance embedded system design has been the subject of many books (e.g., [2]). The
126 functionality design of this UAS is thus beyond the scope of the paper and will not be further elaborated.
127 Instead, we describe some general security-related considerations on the selection of processing
128 elements (i.e., the CPU and FPGA). The processing elements must be chosen to securely deliver the UAS
129 functionality requirements. This UAS application involves sophisticated signal processing and requires
130 high throughput (e.g., measured by the number of floating point operations per second) with a stringent
131 SWaP allowance.

132 In order to support a complicated signal processing algorithm, the CPU will need large memory and
133 storage. The choice of a popular "mainstream" processor will allow the leverage of available software
134 libraries in application development, but it may not have the security features desired for the CONOPS.
135 On the other hand, a "secure" processor with built-in security features may simplify system
136 development, but it may not possess the appropriate processing power or may not support large
137 memory space required for the application. Besides, system openness and upgradability must be
138 considered before choosing a secure processor over a mainstream CPU.

139 Lincoln Laboratory has developed and demonstrated a secure embedded system architecture that uses
140 a security co-processor (S-COP) to secure a mainstream CPU. We will describe this technology later in
141 this paper.

142 Many popular FPGAs are built with embedded security features [4]. FPGAs should be selected on their
143 capability to encrypt and authenticate their configuration bit-streams, incorporate security monitors to
144 detect attacks, and erase decryption keys to protect the CPI, in this case its firmware, when attacks are
145 detected. Ideally, the FPGA design flow should allow some level of fault containment and tolerance by
146 using modular redundancy, watchdog alarms, security level segregation, and test logic (e.g., the IEEE
147 1149.1 Standard Test Access Port and Boundary-Scan Architecture) disabling.

Threat Analysis

149 Adversaries want to sabotage U.S. missions and/or develop counter-measures. The first step in
150 designing a secure system is to analyze the potential attacks that the system may be subjected to when
151 it is deployed. Its CONOPS determines not only functional requirements, but also potential attacks of an
152 adversary. The attacks depends on the adversary capability (e.g., a nation-state) and its attack objectives
153 (e.g., to exfiltrate CPI). In the UAS example, we assume that there is a high probability of equipment loss
154 due to the small UAS size and its use in hostile areas. The UAS attack tree example in Figure 4 describes
155 three logical attack surfaces: boot process, system data, and software, and one physical attack surface:
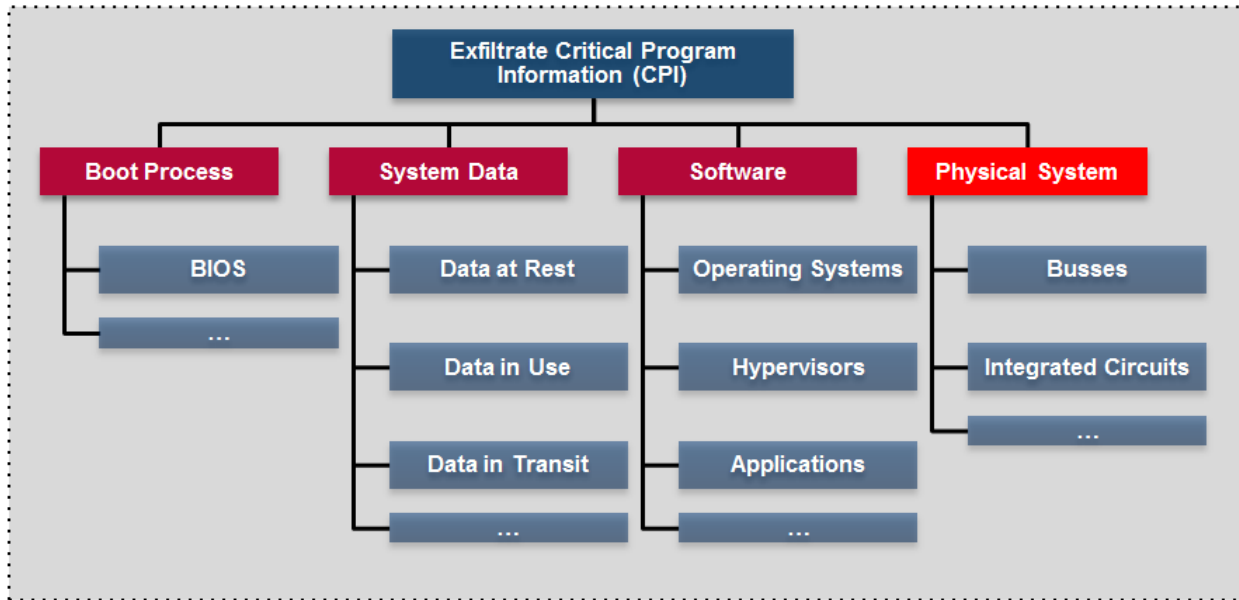156 physical system, against which adversaries may attack to exfiltrate CPI.

157

158 **Figure 4: Example UAS attack tree.**

159 A secure system must establish a root of trust when it starts. The CPU boot process is thus the
160 foundation of a secure embedded system and must be protected from attacks on its confidentiality and
161 integrity. Current practice uses a trusted platform module (TPM) to authenticate software components
162 [5]. A TPM offers facilities for the secure generation of cryptographic keys and limitation of their use. It
163 also includes capabilities such as remote attestation, encryption, decryption, and sealed storage. A
164 software application can also use a TPM chip to authenticate hardware devices. Since each TPM chip has

165   a unique and secret key burned in as it is produced, it is also capable of performing platform
166   authentication.

167   TPM, being a commercial product, made a number of compromises to ensure adoptability by cost-
168   averse vendors and privacy concerns of the general public. The manufactured parts had to be
169   inexpensive and cause as little disruption to the current processing architecture. Additionally, privacy
170   concerns forced that the use of the device to be an optional and passive part of the processing system
171   operations. These compromises led to a low performance device without adequate physical protection.
172   In the next section, we will introduce Lincoln Laboratory's S-COP security coprocessor equipped with a
173   physical unclonable function (PUF), which was developed to address the TPM's inadequacy in tactical
174   operations.

175   Alternatively, the latent vulnerability (e.g., bugs) within an authorized software component (e.g., from
176   open source) may be exploited to compromise system operations. Adversary may exploit these
177   vulnerabilities to access critical data or gain control of the platform itself. Even though when only
178   authorized users are allowed to access the system, threats could come from the introduction of
179   untrusted software (e.g., malware) or unwanted functionality through a third party's intellectual
180   property (IP), either through malfeasance or negligence. A secure system must prevent compromised
181   software from giving an attacker unfettered system access. Commercial systems are starting to address
182   these issues. Software developers use separation kernels to establish and isolate multiple partitions and
183   control information flow between these partitions. On the hardware side, for example, Intel has been
184   developing a Secure Guard Extensions (SGX) that enforces separations between threads executing on
185   the same processor [6].

186   Since the UAS is built with minimal system software for dedicated purposes, the exploitation of software
187   vulnerability may be less likely than a general-purpose computer. The strictly controlled provisioning
188   environment accessible by a very limited number of authorized users also reduces the risk of introducing
189   unverified and/or untrusted software to the UAS.

190   One should always assume that an adversary will attempt to eavesdrop on the UAS data. For example,
191   as the UAS communicates wirelessly, an adversary could potentially eavesdrop on the communication.
192   Data protection is thus a high priority for a secure processor. We need to protect the confidentiality and
193   integrity of the UAS data existing in three forms: data-in-use, data-at-rest, and data-in-transit. Various
194   hardware and software cryptographic solutions, for example, self-encrypting drives[1] and HAIPE (High
195   Assurance Internet Protocol Encryptor), are available. However, the challenge is that encryption must be
196   fully integrated with the processor for efficient performance and protection. Also, the effectiveness of
197   encryption depends on its key management. We will explain an embedded system security framework
198   that is based on the Lincoln Open Cryptographic Key Management Architecture (LOCKMA) library.

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[1] Self-encrypting drives, commonly used in laptop protection, are not adequate for classified information
protection.

199 Physical attack is a particular threat to tactical systems. The UAS needs to consider physical attack since
200 there is a higher probability for adversaries to gain physical access to the device, e.g., by capturing it.
201 One must then assume that the adversary could have an extended period of time to reverse engineer
202 the system. The adversary may want to modify or reverse engineer sensitive system components.
203 Protection against physical attack is also required in foreign military sales (FMS). Like an adversary, a
204 foreign nation may attempt to explore the system that it has purchased, either to leapfrog its own
205 technology, or to gain unauthorized capabilities. The most popular technique to date is to use a
206 protective enclosure to delay unauthorized accesses, which has to deal with the challenge of
207 maintaining standby power for intrusion detection and responses.

Security Metrics

209 In this section we define a few security metrics for evaluating a system during its design process. One of
210 the challenges in the development of secure embedded systems is the inherent difficulty in
211 quantitatively specifying and measuring security. Based on the CIA triad and usability design principles,
212 we have created three practical security metrics to facilitate the design of a secure embedded system:

213 Trustworthiness - a qualitative measure of the system's effectiveness in defending against potential
214 threats relevant to its CONOPS. Based on the current system design and the confidence in the fidelity of
215 that information, one can develop a certain level of trust in its behavior. The fact that a system is
216 equipped with a defense mechanism against a certain threat apparently improves its security and thus
217 trustworthiness. However, while unprotected vulnerabilities reduce security, it is valuable to understand
218 the current system's vulnerabilities; one can apply the protection metric (described next) to improve the
219 design by supporting "added-on" protection technologies to address its vulnerabilities.

220 Protection - a qualitative measure of the system's capability to support "added-on" protection
221 technologies and address vulnerabilities in a CONOPS. The system security can be expressed as a
222 function of the trustworthiness and protection metrics, as they together gauge its security,
223 vulnerabilities, and protection.

224 Usability - a qualitative measure of the system's suitability for a particular CONOPS. A system that is
225 highly secure but incapable of delivering the required functionality is nevertheless not a valid design.
226 This metric evaluates a system design by considering its throughput, portability, upgradability, SWaP
227 (size, weight, and power) and other similar parameters.

228 These security metrics do not support absolute measurements, but provide parameters to guide the
229 design of security into an embedded system as its mission functionality architecture evolves. In addition,
230 multiple system architectures can be qualitatively evaluated and compared to determine relatively how
231 well they provide security. As these metrics are by nature qualitative and subjective, sufficient
232 documentation of justification must be kept for each decision made.

233 The processing requirements, threats and protection needs of a system do not stay constant over the
234 course of its operation. We thus define four operational phases for a secure embedded system so that it
235 can be evaluated accordingly:

236 Startup – In this phase, a system is being "booted" into a state suitable for operations. A Trusted
237 Computing Base (TCB), which defines the components being trusted for security, is established.

238 Execution – The system is in the state of operation and performs functions required by the mission.

239 Shutdown – In this phase, the system is in the process of turning off.

240 Off – The system has been powered down.

Secure Embedded System Architecture and Enabling Technologies

242 As mentioned, the CPI of a commercial-off-the-shelf (COTS) based embedded system is mostly in its
243 software and firmware so encryption is the foundation of its overall security. There are many efficient
244 and iron-clad secure cryptographic primitives, such as the NSA approved Suite B cryptography [7]. These
245 primitives can be implemented with software, firmware, or hardware, and can often be obtained as
246 open-source IPs (intellectual properties). However, simply using "standard" cryptographic primitives
247 cannot guarantee the adequate implementation of security functions. The manner that the
248 cryptographic primitives are assembled and coordinated into the desired application-specific security
249 functions is critical to their effectiveness. Also, encryption effectiveness depends on key management,
250 which includes the generation, distribution, and protection of keys.

251 Lincoln Laboratory has developed a solution to address these challenges. Lincoln Laboratory Open
252 Cryptographic Key Management Architecture (LOCKMA) is a highly portable, modular, open software
253 library of key management and cryptographic operations that are suitable for embedded uses. Designed
254 to secure a wide range of missions, it provides user, identity, and key management and supports for
255 hardware and software cryptographic primitive kernels. LOCKMA's frontend application programming
256 interface (API) provides application developers with a simple and intuitive access to LOCKMA's core
257 functionality. Figure 5 summarizes LOCKMA's interfaces to high level security functions and low level
258 crypto primitives. To use LOCKMA, developers are not required to have advanced knowledge of the
259 cryptography or key management algorithms implemented by LOCKMA's core modules. These modules
260 handle the processing of key management messages. They make extensive use of cryptographic
261 primitives available in several commercial and Open Source libraries.
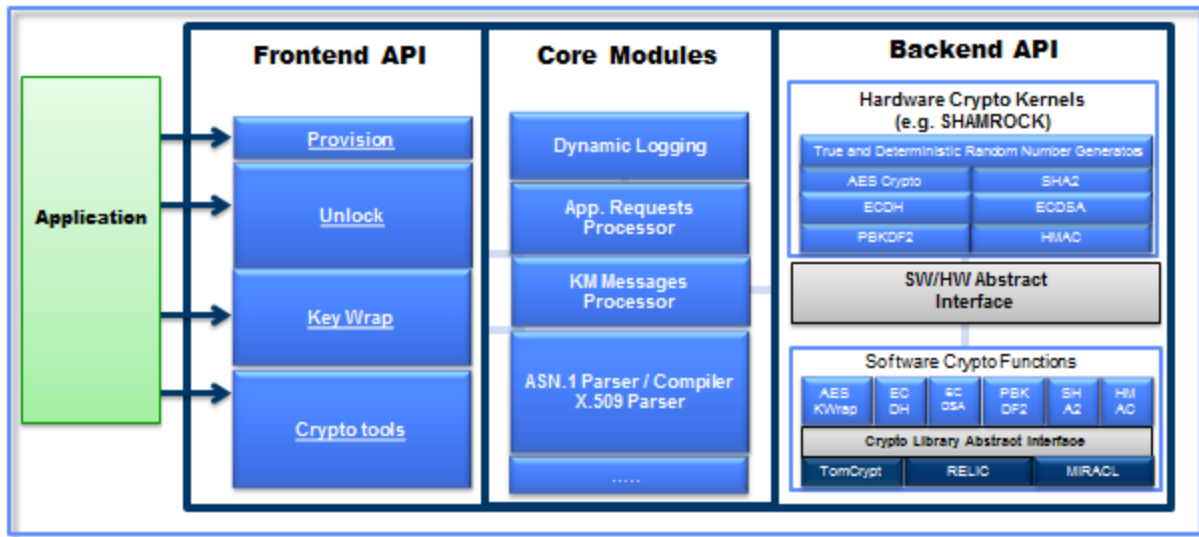
Figure 5: LOCKMA provides application interface, high level security functions, and low level cryptographic kernels.

Lincoln Laboratory has implemented LOCKMA in a security coprocessor (S-COP), which implements cryptographic primitives in hardware. The added benefits of hardware implementation include much faster computation times, lower power use, and hardware separation and protection of sensitive keys from non-sensitive data and code. We have demonstrated the use of S-COP to secure an embedded system.

Figure 6 shows the UAS embedded system architecture in which the CPU secured with an S-COP and a physical unclonable function (PUF). The S-COP employs dynamic key management and accelerated Suite B cryptography for the measurement and verification steps necessary to securely boot the CPU. The PUF provides an inviolable root-of-trust, from which a unique cryptographic key is derived.

Figure 6: An S-COP is used along with a PUF to secure a COTS CPU.

Lincoln Laboratory has adopted an optical PUF, which can be implemented on a fully fabricated printed circuit board (PCB). As illustrated in Figure 7, the PUF is constructed by adding one or more light emitting diodes (LEDs) and an imager to the PCB, which is then coated with a thin polymer planar

10

279　waveguide. Upon power-up, the S-COP derives a unique value from the imager, which receives light
280　emitted by the LEDs and travelled through the waveguide. This value is then used for identification and
281　key derivation. Manufacturing variations ensure a unique identification value for each board. Invasive
282　attempts to learn about the PUF value (e.g., for cloning purposes), even when the PCB is unpowered,
283　will disturb and damage the coating and irreversibly destroy the PUF value. Cloning and other
284　unauthorized actions are thus prevented.

285

Figure 7: Optical PUF implemented with a waveguide; (a) operating concept illustration, (b) implementation on a fully fabricated PCB.

288　Many factors, for example, temperature, aging, etc., can cause the image to vary. A technique called
289　fuzzy extraction is employed to ensure that the same key will be derived from the PUF under various
290　situations [8]. This ability allows the S-COP to secure the boot process, load only trusted software, and
291　ensure that the unique identity is intact, before, during, and after boot process. In addition to protecting
292　data-at-rest with cryptography, the S-COP also uses key management to support secure communications
293　between subsystems to protect data-in-transit.

294　This architecture allows software applications to be developed and tested initially without invoking
295　security features. When a system is provisioned for deployment, the PUF is applied to its PCB and the
296　finalized software code encrypted with the PUF derived key is loaded. The system will not start if its PUF
297　value is incorrect, causing a failed software decryption. The decoupling of the S-COP and the CPU allows
298　DoD systems to leverage mainstream CPUs, enhancing their performance, usability, and upgradability.

299　Figure 8 shows a testbed that we have developed to evaluate the S-COP-based secure architecture. In an
300　unsecured architecture, the CPU reads in the basic input output system (BIOS), and bootstraps the
301　operating system (OS). Without authentication, the CPU is vulnerable to maliciously modified BIOS and
302　OS. The S-COP-based secure architecture addresses this vulnerability by authenticating the BIOS, OS and
303　applications, which is illustrated in Figure 9. When the system powers up, the S-COP halts the CPU while
304　it performs authentication. It first reads the PUF and derives a key. The key is used to decrypt the BIOS.

11

305 If successful, the CPU is released to execute the BIOS. The SCOP then authenticates and decrypts the OS,
306 and boots the system up. Encrypted applications are loaded and handled in the same manner. In
307 addition to associating an application with a specific system, the system can use LOCKMA dynamic key
308 management to dynamically and seamlessly adjust the authorization of application execution (e.g., in
309 time-specific and/or location-specific modes). Figure 10 illustrates the data protection functions of the
310 S-COP, which uses LOCKMA to set up secure encrypted communication channels between multiple
311 systems as well as encrypt the storage (data-at-rest).

312

313

314 **Figure 8: A secure processor integrating a CPU, an S-COP, and a PUF.**
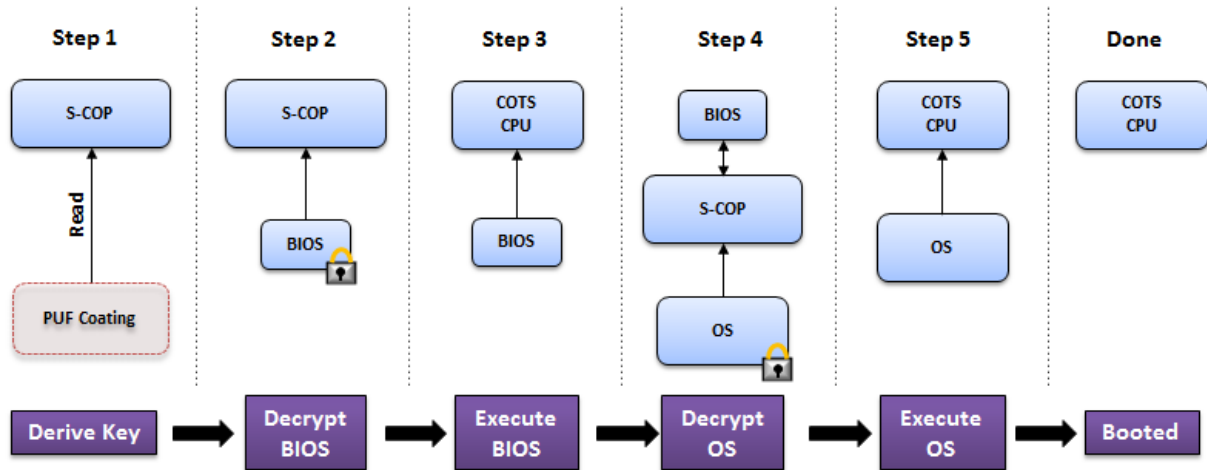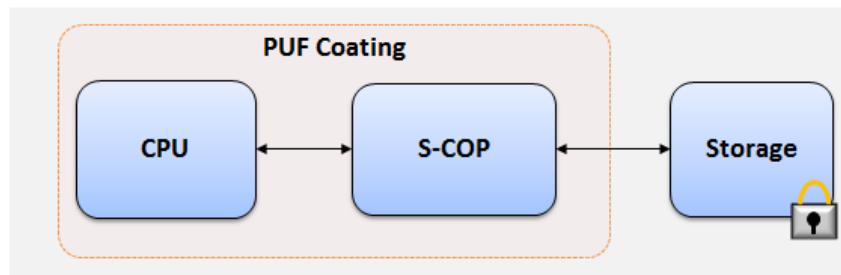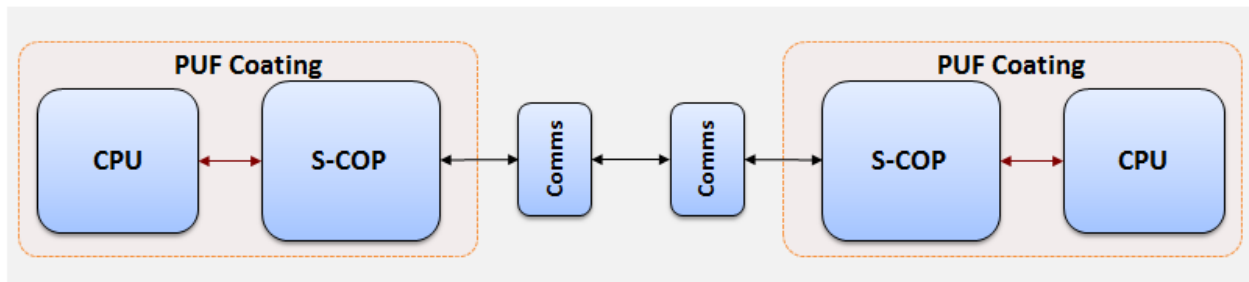
315

Figure 9: Secure boot process. The CPU is halted until S-COP successfully verified system integrity.

(a)

(b)

Figure 10: Data protection of (a) data-at-rest; (b) data-in-transit.

Evaluation

In terms of the CIA triad, the S-COP addresses confidentiality and integrity by protecting the boot process, data, and communication from unauthorized access and alternation. The S-COP itself does not ensure a system's availability, but it can be adapted to support other agility and resilient measures such as moving target technologies [9].

328 As an example, we evaluate the hypothetical UAS embedded system, after adopting the S-COP-based
329 secure architecture, using the three security metrics: trustworthiness, protection, and usability. A
330 mainstream unsecured CPU by itself receives low trustworthiness ratings during all system operation
331 phases as we assume that it needs an inherently large TCB and lacks hardware enforced boot attestation.
332 The security of such a CPU enhanced with S-COP dramatically increases across all system operation
333 phases, earning it higher trustworthiness ratings. However, during the execution phase, one still needs
334 to trust the operating system, which may have inherent vulnerabilities. The trusted boot does not
335 completely eliminate the risk of running untrusted/unverified codes that could potentially escalate
336 privileges or exfiltrate information.

337 If a CPU has no explicit support of volume protection, it will receive low protection ratings during the
338 boot phase. The integration with a TPM provides key storages and measurements. However, any usage
339 of these keys still requires the operating system to handle them properly, thus increasing the TCB. A
340 lack of overall support for physical protection or hardware enforced encryption of code and data allows
341 for snooping or modification of memory during the execution phase. During the off phase, the TPM
342 could be physically replaced and thus a new set of measurements could be inserted into the system. The
343 S-COP-based secure architecture mitigates these deficiencies by creating a root of trust with a PUF and
344 can be used to support volume protection.

345 Since the S-COP can be adapted to secure a mainstream CPU, the usability of the secure UAS embedded
346 architecture rates high as it can leverage all the benefits of a COTS CPU, such as high performance (e.g.,
347 for signal processing), large cache and memory support, and widely supported software libraries.

348 ## Open System Architecture Security

349 As military electronic systems continue to increase in sophistication and capability, the cost and
350 development time of these systems also grow. The use of open system architecture (OSA) can improve
351 the development and lifecycle efficiency of asset procurements. Typically OSA incorporates several
352 buses with well-defined interfaces for communications (controls and data) between components. The
353 system can then be adapted to different functionality by providing proper components and defining
354 their interconnections.

355 Besides the securing of a CPU, LOCKMA is being developed into a crypto-based secure framework that
356 has been successfully demonstrated in OSA embedded system protection. The framework employs
357 LOCKMA, e.g., in the form of collaborating S-COPs, to provide encryption of data-in-use, data-in-transit,
358 and data-at-rest to countermeasure eavesdropping, probing and unauthorized accessing. In addition, a
359 trusted configuration is enforced by extending the secure boot concept and accepting only
360 predetermined payloads and preventing unauthorized hardware and/or software substitute. An
361 example configuration illustrated in Figure 11 consists of several payloads and processors and a LOCKMA
362 security manager (LSM). The authorized mission configuration is specified by a digitally signed "config
363 file" that specifies authorized payloads, allowed combinations of payloads, and secure communication
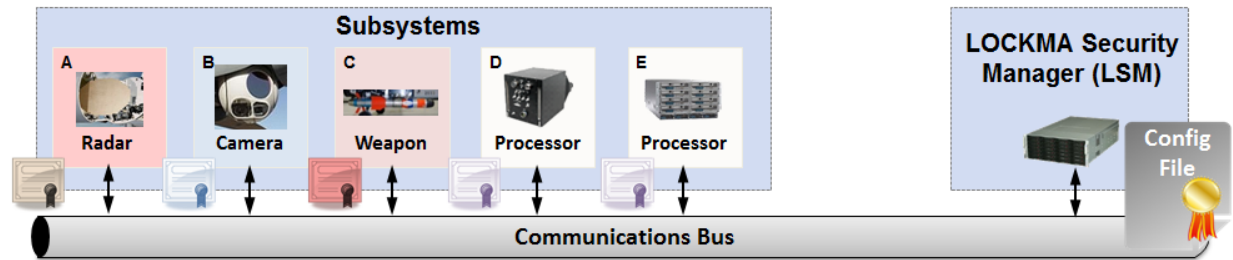364 channels.

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Figure 11: In a LOCKMA-based OSA security framework, LSM checks subsystem credentials against a config file to ensure that the configuration is authorized.
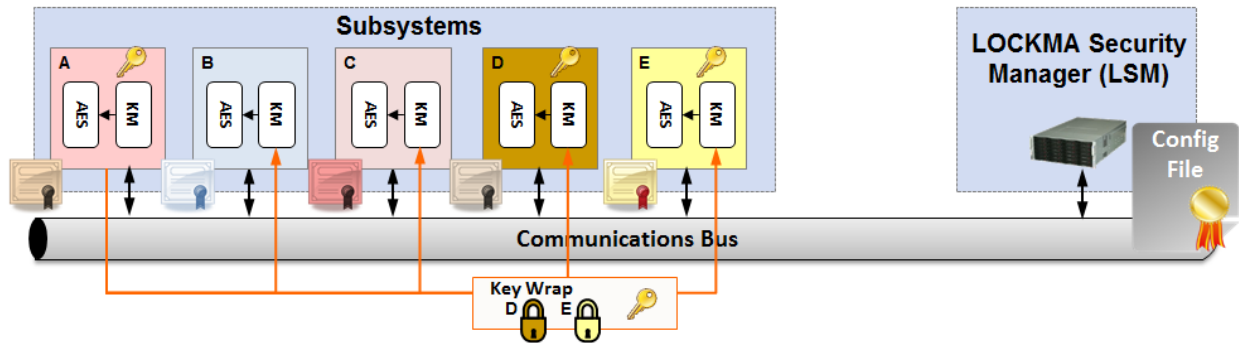

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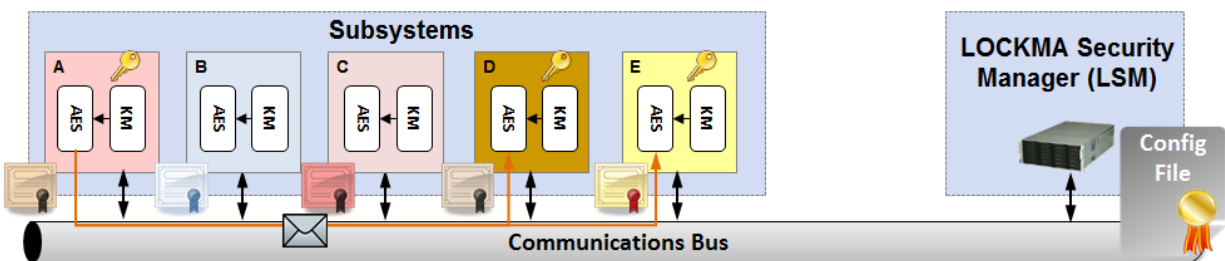
Figure 12: Security configuration file for enforcing payload authorization and securing communication channels.

At start-up, the LSM verifies the digital signature of the config file and ensures that it is unaltered. Using the config file, the LSM collects subsystem credentials and confirms that the system has no unexpected payloads and its configuration (i.e., component combination) is authorized. The system now starts and the LSM continues to set up secure communication channels. Figure 13 illustrates that each subsystem is provided with, e.g., by embedding an S-COP, a key management function (KM) and an AES (advanced encryption standard) encryption/decryption function. Subsystem A creates a key wrap containing a symmetric crypto key that is only accessible by authorized subsystems D and E, and establishes a communication channel. The channel users retrieve the common secret session key and use it for encrypted communications. The system is now ready to perform its mission objectives.

380

381   (a)

382

383   (b)

384   **Figure 13: In a LOCKMA security framework, (a) subsystem A sends a key wrap openable only by**
385   **subsystems D and E to retrieve a session key, and (b) all three subsystems are then enabled to carry**
386   **out encrypted communication.**

Ongoing Work

Security is of asymmetric nature as an attacker can render any system defense useless by discovering a single, unexpected vulnerability. As it is impossible to correctly predict every future attack, securing an embedded system to prevent it from being attacked is not a guarantee of mission assurance. Just being secure is no longer adequate, systems must also be resilient. Lincoln Laboratory is vigorously pursuing an answer to the essential mission assurance question: "What can be done if the attacker is successful despite the best practice to provide security?"

Our objective is to define a standardized, reference security and resilient architecture for future DoD embedded systems. We want to ensure that the system continues to function when things do not go as we expected. Our work is guided by the four stages of actions involved with the resiliency of an embedded system: anticipate, withstand, recover, and evolve [10]. Our current R&D effort focuses on approaches that enable a system to withstand attacks and complete mission goals, recover from a degraded state back to a nominal state, and evolve to improve defense and resiliency against further threats.

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